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Abstract:

This deliverable specifies the hardware extension and MAC upgrade for the MIMO testbed. Further, it defines a road map for implementing the hardware extension and defines a date for its completion (Milestone M2.3.1). It also provides some details on the planning for M2.3.2.

Contents

1	Description of the MASCOT MU-MIMO Testbed	5
1.1	Real-Time MU-MIMO Testbed	5
1.1.1	Phase-1 PHY/MAC Extensions (M2.3.1)	6
1.1.2	Phase-2 MU-MIMO Testbed Extension	7
1.2	Non Real-Time MU-MIMO Demonstrator	7
2	MU-MIMO Extensions to the ETHZ MIMO Testbed	9
2.1	The ETHZ MIMO-OFDM Testbed	9
2.1.1	PCI-Based FPGA Platform	10
2.1.2	Analog RF Frontend	10
2.1.3	Software Stack	11
2.2	MIMO Testbed Hardware Extensions	12
2.3	MIMO Testbed PHY and MAC Extensions	14
2.4	Non Real-Time MU-MIMO Testbed	19
3	Testbed Extension Summary and Roadmap	20
3.1	Tasks and Milestones	21
3.2	Risk Analysis	22

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Executive Summary

The aim of Task 2.3 of the MASCOT project is the development, testing, and demonstration of multi-user (MU) MIMO algorithms. This deliverable describes the status of this work, the implemented setup, and the planning of the work ahead. A summary of the corresponding milestones and the updated time line are provided in Fig. 1. The testbed setup to be used

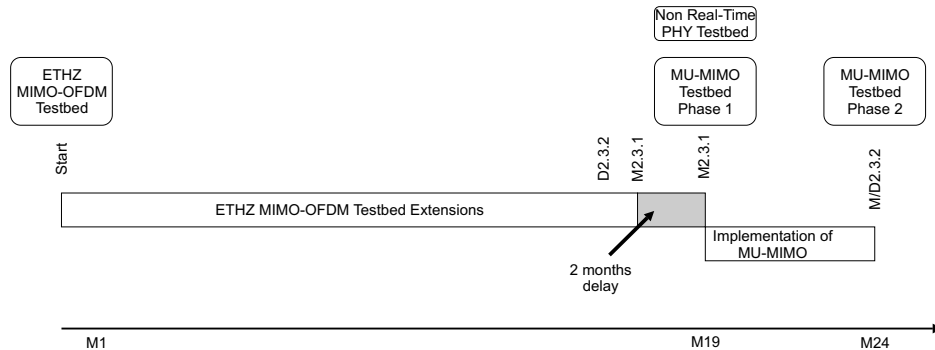


Figure 1: Overview of planning for the development of the MASCOT MU-MIMO testbed

within MASCOT is comprised of two components: A real-time MAC/PHY testbed which is based on the ETHZ MIMO-OFDM testbed [4] and a PHY testbed for real-time over-the-air transmission with offline processing.

The development of these testbeds is partitioned into two phases: The first phase is concerned with the preparation of the hardware. The milestone which marks the completion of this first phase will be reached with two months delay (31.07.2007 instead of 31.5.2007). The real-time demonstration setup reached at the end of this phase will be comprised of three terminals. The second phase of the project is concerned with the implementation of MU-MIMO algorithms on the real-time testbed. The corresponding setup to be completed 31.12.2007 (M2.3.2) will be comprised of 5 terminals and will be based on an extended hardware platform compared to the one used in the first phase of the project.

Chapter 1

Description of the MASCOT MU-MIMO Testbed

1.1 Real-Time MU-MIMO Testbed

The real-time MU-MIMO testbed used within MASCOT is based on the ETHZ MIMO-OFDM point-to-point testbed [4] described in Sec. 2.1. The setup to be developed as a basis for implementing and testing MU-MIMO algorithms is illustrated in Fig. 1.1. The final system is comprised of five identical modems. Each modem employs a MIMO-OFDM PHY layer with four transmit and four receive antennas with support for 20 MHz communication bandwidth. This PHY layer is loosely based on that of the IEEE 802.11n standard, but it deviates from the standard in a number of details which (in the testbed) are designed to simplify the system architecture to be better suited as a research platform for MU-MIMO algorithms. The baseline system also provides some basic MAC layer functions as the basis for the testing of MU-MIMO MAC-layer algorithms such as scheduling, rate adaptation, and precoding. These functions are implemented on a PowerPC processor and on some dedicated support logic which are both tightly integrated with the PHY layer. The corresponding system design ensures low-latency communication between the MAC and the PHY layer and provides full access for the MAC layer to all relevant PHY layer parameters (e.g., SNR, received signal strength, and channel estimates).

The rationale to implement most of the MU-MIMO MAC layer functionality in software rather than completely in hardware is that it is expected that the performance of a software-programmable architecture is sufficient to test relevant MAC layer algorithms such as rate-adaptation and MU scheduling. The advantage of such a mostly software-based MAC architecture is that

it provides the highest degree of flexibility in terms of algorithm development and that it considerably simplifies the integration and testing of new algorithms.

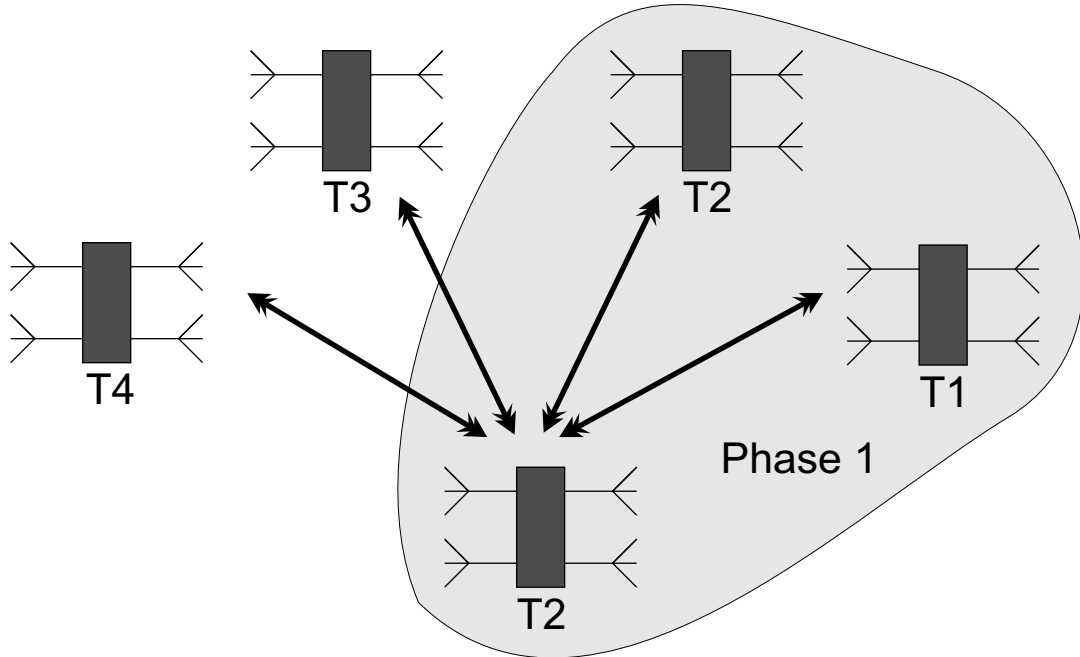


Figure 1.1: Overview of the MU-MIMO testbed baseline setup for real-time demonstrations. The shaded area represents the setup to be realized within Phase 1 of the project (M2.3.1).

1.1.1 Phase-1 PHY/MAC Extensions (M2.3.1)

The first step in the development of a MU-MIMO demonstrator for the MASCOT project is to provide a framework for implementing and testing MU-MIMO algorithms. In addition to the ETHZ MIMO-OFDM testbed, the corresponding system to be used within MASCOT provides a low-complexity RF, a bidirectional MIMO-OFDM PHY layer, and a hardware infrastructure suitable as a basis for a real-time MU-MIMO MAC implementation and a corresponding MAC API which constitutes the basis for the development of the MU-MIMO MAC. This API allows to send and receive data and acknowledgment packets, check the CRC of a received packet, and to assess the status of the transmission medium for channel access control. Moreover, it provides various timers and interrupts to control the frame-timing. Each modem can either serve as a terminal in a decentralized system configura-

tion or as either terminal or base station in a centralized setup. The initial demonstration is done in a configuration with three modems. One modem acts as a base-station, serving two other devices acting as terminals under the control of a MAC with a centralized scheduler.

1.1.2 Phase-2 MU-MIMO Testbed Extension

The second generation real-time MU-MIMO testbed is comprised of five identical modems as illustrated in Fig. 1.1. The PHY, MAC, and RF of these modems are based on the first generation system, outlined above. However, the PHY and MAC layers will be integrated on a new hardware platform. As opposed to the initial development platform, this second generation setup will be the basis for the MU-MIMO demonstrations to be performed within MASCOT (M2.3.2). The redesign of the hardware is necessary, since the original platform contains components which are no longer available, preventing the replication of the system to construct scenarios with more than three modems. The corresponding redesign of the hardware platform addresses the need to substitute these obsolete components and at the same time extends the available hardware resources for MU-MIMO extensions by using larger FPGA devices compared to the first generation platform. Moreover, this system has provisions to add a daughter board with a PHY layer ASIC and to use all FPGA resources for the implementation of a corresponding MAC layer.

1.2 Non Real-Time MU-MIMO Demonstrator

The real-time MU-MIMO demonstrator described above has a considerable complexity (especially at the PHY layer) and the need to meet stringent real-time requirements for the signal-processing makes the integration and testing of new algorithms a time-consuming task. Hence, it is advisable to focus on MAC-layer algorithms and on the most promising PHY-layer algorithms which require real-time operation (e.g., feedback of channel state information) for real-time demonstrations. Algorithms which require no real-time processing can be tested and demonstrated under real-world conditions using a combination of real-time transmission with offline signal-processing. A suitable test setup is illustrated in Fig. 1.2.

The corresponding testbed uses MATLAB as a tool for implementing MU-MIMO coding and baseband digital signal processing algorithms. Real-time transmission and reception is performed on a frame-by-frame basis using a

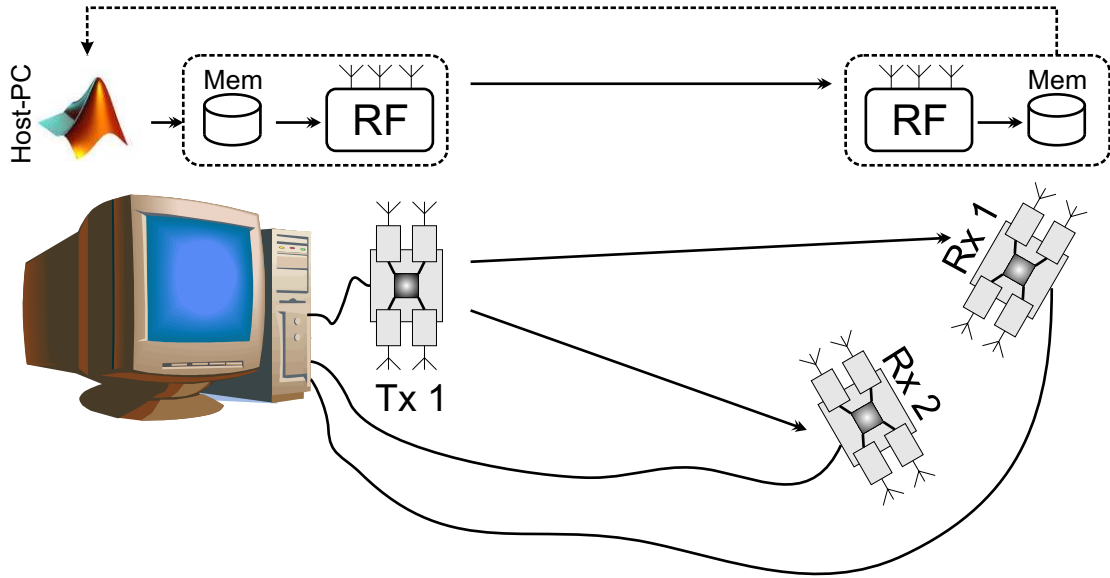


Figure 1.2: Non real-time Phase 1 MU-MIMO testbed setup for assessment of real-world link and PHY characteristics.

combined FPGA/RF platform [2] which supports narrowband or wideband transmissions with up to 40 MHz bandwidth.

The final setup will be comprised of up to five identical terminals. The first application of the setup is the comparison of different transmission schemes, including spatially-multiplexed Alamouti codes, Golden codes [5], MU-STBCs developed in [3], and straightforward spatial multiplexing.

Chapter 2

MU-MIMO Extensions to the ETHZ MIMO Testbed

2.1 The ETHZ MIMO-OFDM Testbed

An overview of the hardware architecture of the ETHZ MIMO-OFDM testbed [4] is provided in Fig. 2.1. The setup, which constitutes the basis for the MASCOT MU-MIMO testbed, supports a *unidirectional* point-to-point link under the control of a PHY-layer API which is implemented in MATLAB on a host-PC. This API allows to conduct PHY-layer measurements, but is not well suited as a basis for the implementation of a MAC layer (mainly due to increased communication latencies on the PCI bus between the host-PC and the PHY layer, and due to the absence of embedded processor resources appropriate for MAC layer processing).

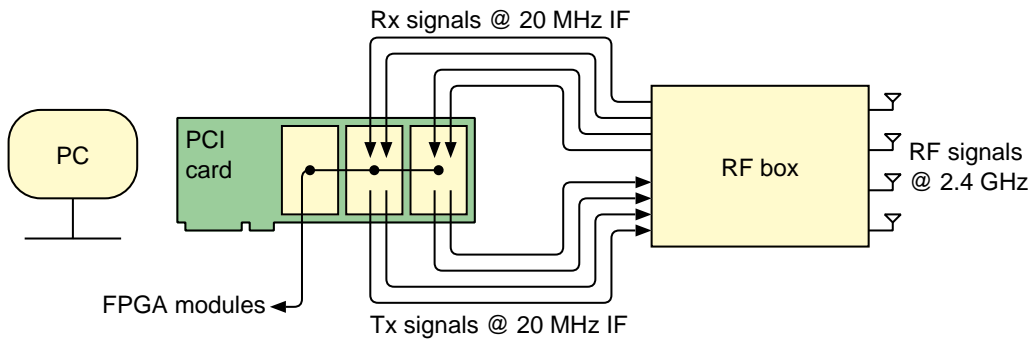


Figure 2.1: Schematic overview of the ETHZ MIMO-OFDM testbed

2.1.1 PCI-Based FPGA Platform

The employed PCI platform, shown in Fig. 2.2, hosts three hardware modules: a large FPGA (Xilinx XC2V6000-6) module for baseband signal processing and two converter modules for digital-to-analog and analog-to-digital signal conversion. On an FPGA (Xilinx XC2V1000-4) provided on each of the converter modules, the baseband signals are digitally converted to an intermediate carrier frequency (IF) of 20 MHz. Hence, the total number of converters is reduced by a factor of two compared to traditional baseband systems with separate converters for the I and Q components. Incidentally, the digital IF also avoids any I/Q imbalance, however, at the cost of higher sampling rate and resolution. Both the 14 bit digital to analog converters (DACs) and the 12 bit analog to digital converters (ADCs) run at a sampling rate of 80 Msp/s.

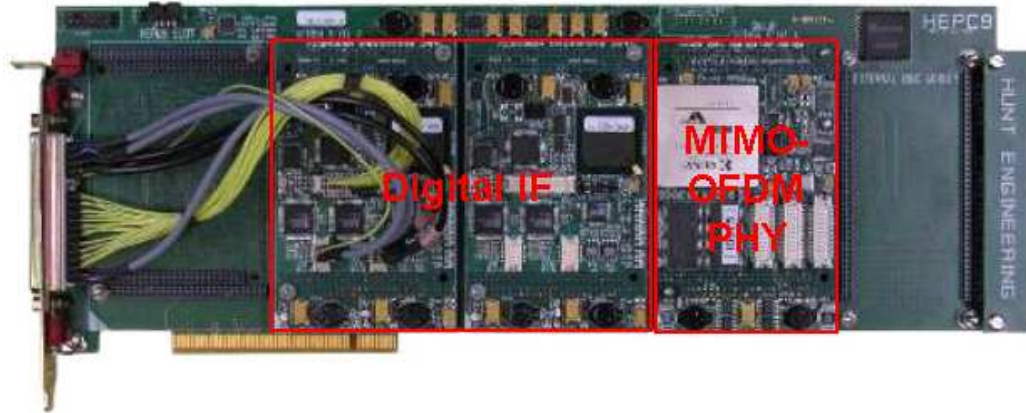


Figure 2.2: Picture of the PHY layer processing platform from Hunt Engineering used for the PHY-layer processing in the ETHZ MIMO-OFDM testbed.

2.1.2 Analog RF Frontend

The RF box associated with each terminal is shown in Fig. 2.3. The MIMO transceiver chain is comprised of four SISO super-heterodyne RF chains with an analog IF of 475 MHz. The chains are built from discrete RF components and support 20 MHz bandwidth channels with center frequencies in the 2.4 GHz ISM band. The received signal power at the ADCs is regulated by digitally controllable analog attenuators. These attenuators extend the dynamic range of the receive chains by 31 dB. In conjunction with the 12 bit

resolution of the ADCs, the useful dynamic range amounts to approximately 70 dB.



Figure 2.3: Picture of the RF box, built from discrete RF components, used in the ETHZ MIMO-OFDM testbed

2.1.3 Software Stack

The testbed is controlled from a host-PC through multiple layers of software that allow communication with the hardware. The software stack includes a hardware driver for the PCI board, a transceiver-specific API that provides several functions (for the digital baseband configuration and the transmission or reception of OFDM frames), and a MATLAB interface (MEX) function to call these API functions. Demo applications, configuration tools, and measurement sequences are programmed as MATLAB scripts.

2.2 MIMO Testbed Hardware Extensions

The schematic of the MASCOT MU-MIMO testbed hardware setup is provided in Fig. 2.4. The goals of this modified setup as opposed to the one used in the ETHZ MIMO-OFDM testbed are to integrate MAC layer hardware together with the PHY layer and to add an integrated RF to enable replication to a multi-user setup.

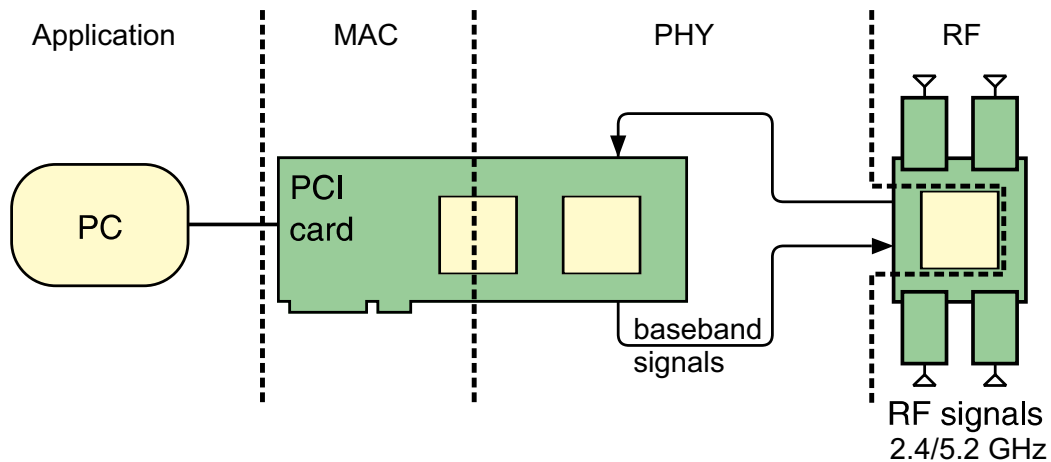


Figure 2.4: Schematic overview of the MASCOT MU-MIMO testbed

PHY/MAC platform The MAC and the PHY layer of the system are both implemented on the FPGAs of the ETHZ *VAMP*¹ prototyping platform [1] shown in Fig. 2.5. The core elements of this prototyping system are two XILINX Virtex-II Pro FPGAs (XC2VP50-5-ff1517) which provide programmable logic resources, integrated multipliers, and each FPGA contains two embedded PowerPC processors. The latter are well suited for the implementation of the MAC layer of the MASCOT MU-MIMO testbed since they can be tightly integrated with the logic of the PHY allowing for low PHY/MAC interface latencies.

RF platform The integrated MIMO RF developed within the MASCOT project is called ETHZ *QuadBAT* [2] and shown in Fig. 2.6. This RF subsystem is built using a modular approach in which up to four SISO chains can be connected to a central carrier board. This carrier board can be connected to the PHY/MAC subsystem. The separation of the individual RF chains ensures modularity and good isolation between the multiple RF chains. Each

¹Virtex-II Pro Astonishing Multi Purpose (VAMP) board

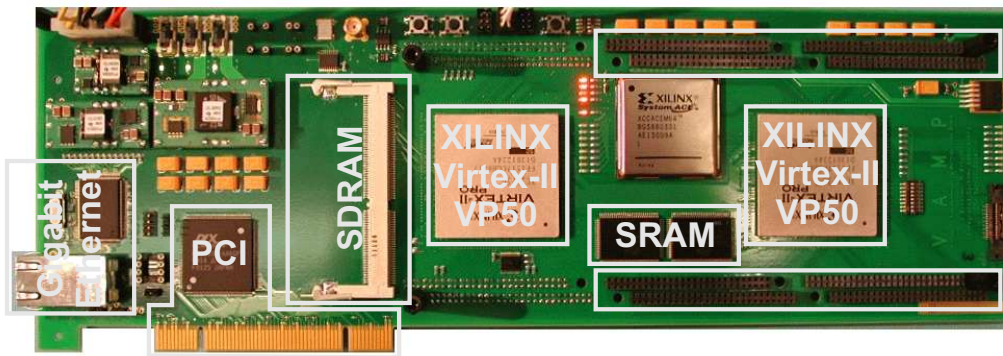


Figure 2.5: Picture of the ETHZ prototyping FPGA platform (VAMP board) [1]

RF chain is built around a MAXIM MAX2829 SISO RF transceiver ASIC for WLAN and supports 2.4 GHz and 5.2 GHz operation with 20 MHz and 40 MHz bandwidth.



Figure 2.6: Picture of the integrated MIMO-RF with additional baseband FPGA carrier (QuadBAT platform) [2]

2.3 MIMO Testbed PHY and MAC Extensions

The high-level block diagram of the MU-MIMO prototyping system for implementation and assessment of 802.11n (MIMO) PHY and MAC algorithms is shown in Fig. 2.7. The overall prototyping system consists of several parts: a host-PC to run application and control software (e.g. MATLAB), an FPGA baseboard carrying two XILINX Virtex-II Pro FPGAs with embedded PowerPCs and several peripheral ICs (VAMP board), and a second, modular FPGA subsystem implementing parts of the MIMO PHY with digital (MIMO frontend) and analog (RF) parts (QuadBAT platform). The VAMP prototyping board connects to the outside world either wired - through a 32 bit PCI bus or a Gigabit Ethernet interface - or wireless - through the QuadBAT FPGA subsystem incorporating also RF components.

The components of the FPGA subsystem are connected through a high-speed on-chip bus - the AMBA² *Advanced High-Performance Bus* (AHB) - for data transfer, and a low-speed on-chip bus - the AMBA *Advanced Peripheral Bus* (APB) - for configuration purposes and status information.

The FPGA prototyping system is designed to incorporate a MIMO PHY, a MU-MIMO MAC, an Ethernet MAC, and a Gigabit Ethernet connection. Most of these blocks are implemented in hardware. However, significant parts of the MU-MIMO MAC and parts of the Ethernet MAC will be implemented in software on the embedded PowerPC processor. The Ethernet interface allows to operate the prototyping system also stand alone without host-PC.

Building blocks which are highlighted orange in Fig. 2.7 need either implementation, adaptation or extension to provide the basis for the MU-MIMO MAC functionality.

PHY interface The interface between PHY and MAC layer had to be defined. The system provides two separate memory buffers, one for the transmit and one for the receive path. These two buffers together with some more functionalities (CRC computation/check, master/slave interfaces, header generation) are complete redesigns compared to the ETHZ MIMO-OFDM testbed.

PHY frontend With the new RF frontend shown in Fig. 2.6 also the PHY needed some adaptations. Digital up- and down conversion is no longer necessary as this task is now already performed by the new analog/RF subsystem. Instead, up- and down sampling and some low pass filtering is necessary.

²AMBA: Advanced Microcontroller Bus Architecture

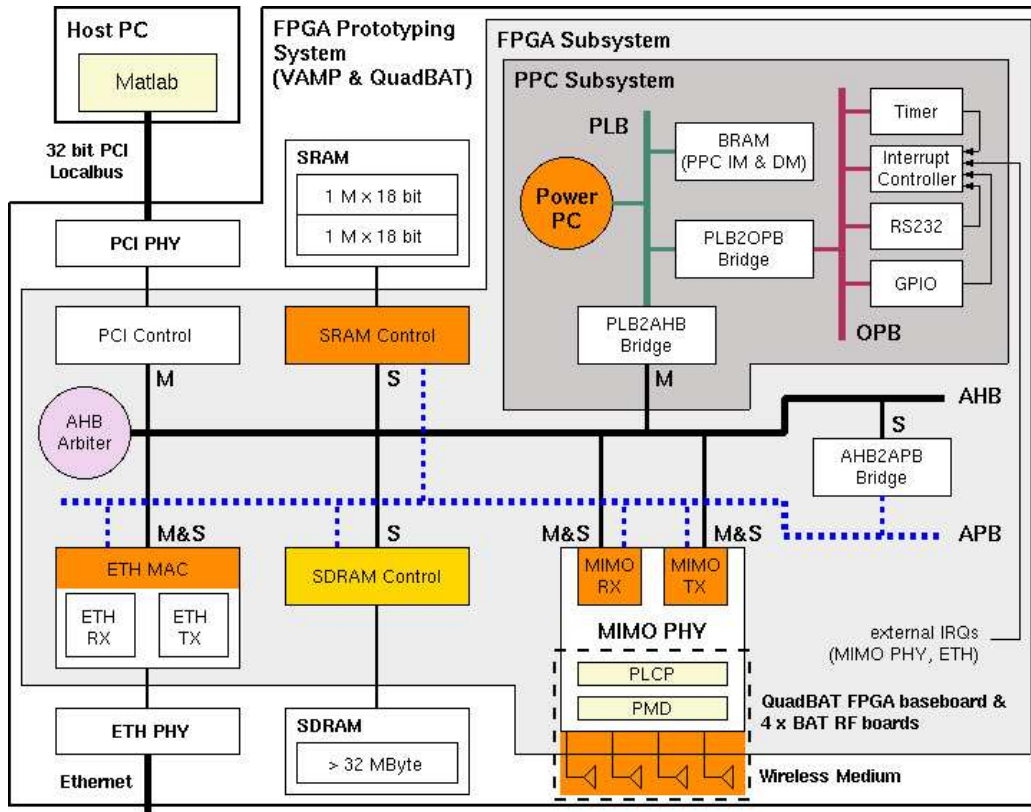


Figure 2.7: Overview block diagram of the MAC/PHY architecture of the MU-MIMO testbed

Furthermore, the automatic gain control (AGC) needs to be adapted to the new frontend as well as the interface to the VAMP board.

Ethernet interface An Ethernet interface with an AHB master interface providing *Direct Memory Access* (DMA) in order to minimize the time for data transfers had to be added. The Ethernet connectivity has been implemented using a dedicated third-party PHY chip supporting 10 Mbit, 100 Mbit and 1000 Mbit transmission modes. A dedicated low-level MAC layer for the communication with the PHY chip has been implemented in the FPGA. The low-level Ethernet MAC is properly operating in both, 100 Mbit and 1000 Mbit modes. The Ethernet link configured to 1000 Mbit mode is intended to be the wired control and data connection for all MU-MIMO modems. This configuration will facilitate demonstrations using standard IP-based software running on the terminal clients.

PowerPC subsystem The PowerPC subsystem consists of an embedded PowerPC 405 CPU core and various configurable components. The PowerPC core itself is implemented as hardmacro on the FPGA die. The remaining components are laid out as configurable IP blocks and designed to use ordinary FPGA resources (slices). Therefore, these configurable IP blocks need FPGA synthesis and resource allocation.

The PowerPC core uses the *Processor Local Bus* (PLB) as central attachment point for the remaining core or peripheral components. The configurable IP blocks involve core components such as Block RAM (BRAM) representing instruction memory (IM) and data memory (DM), and two bridges, the PLB2OPB and PLB2AHB bridge. The peripheral IP blocks are timer, general purpose I/Os (GPIO), serial line (RS232), and interrupt controller.

The PowerPC subsystem is responsible for the entire MAC layer control for both, the 802.11 wireless MAC and the 802.3 Ethernet MAC. The PowerPC subsystem reacts on specific events occurred within the PHY block or the Ethernet low-level MAC (e.g. 'frame available'). These (peripheral) events are signaled as external interrupts to the interrupt controller within the PowerPC subsystem. The interrupt controller then signals these events through a centralized and direct connection to the processor core. The PowerPC can also be interrupted by programmable or periodic interrupts (programmable/fixed interval timers), which might be suitable for the coordination function within the MU-MIMO MAC.

Memory The external SRAM memory is used to manage the transmit and receive queues. Entire frames (header and payload) are stored there, while the PowerPC only needs to know the frame header information to manage the frames. The memory is connected to the AHB bus and has an AHB slave interface, which will be the target of DMA transfers initiated by different AHB masters, for instance AHB masters of the Ethernet MAC or of the MIMO PHY-layer RX/TX buffers.

MAC Functionality There exist two different MAC entities in this baseline setup: a 802.3 Ethernet MAC and a 802.11 wireless MU-MAC. Both MAC entities are mainly implemented in software and running on the embedded PowerPC. The Ethernet MAC is in charge of handling all incoming and outgoing Ethernet traffic. The MU-MIMO MAC deals with the wireless traffic and has control of the MIMO PHY block. Its long-term architecture is based on the MAC layer features of the IEEE 802.11n standard. The communication between the wired Ethernet MAC and the wireless MAC is handled by the data queues located in the external SRAM.

The bring-up version of the MU-MIMO MAC will employ a simplified *Point Coordination Function* (PCF) operated by a single modem (central arbiter) in order to have a well-controlled environment with strictly scheduled access for initial multi-user communication. Later, more advanced MU-MIMO MAC versions may have a hybrid coordination function, a compound of *Distributed Coordination Function* (DCF) and PCF, and might also include support for *Short Interframe Spaces* (SIFS), *PCF Interframe Spaces* (PIFS), *DCF Interframe Spaces* (DIFS), and *Extended Interframe Spaces* (EIFS). It must be noted, that the wireless MAC (and especially its error handling capabilities) must be designed rather robust in order to cope with ordinary WLAN/ISM interference. A modular, layered software architecture is planned to ease future extensions of the MAC functionality.

MU-MIMO Frame Structure The PHY-layer frame format for MU-MIMO transmission - including beamforming mode - to several clients concurrently is shown in Fig. 2.8. Different headers are foreseen to support various kinds of transmission modes. This draft concept provides the basis for discussions about MU-MIMO transmission scenarios (and demonstrations) and sketches also some impacts of important architectural decisions for both, hardware and software.

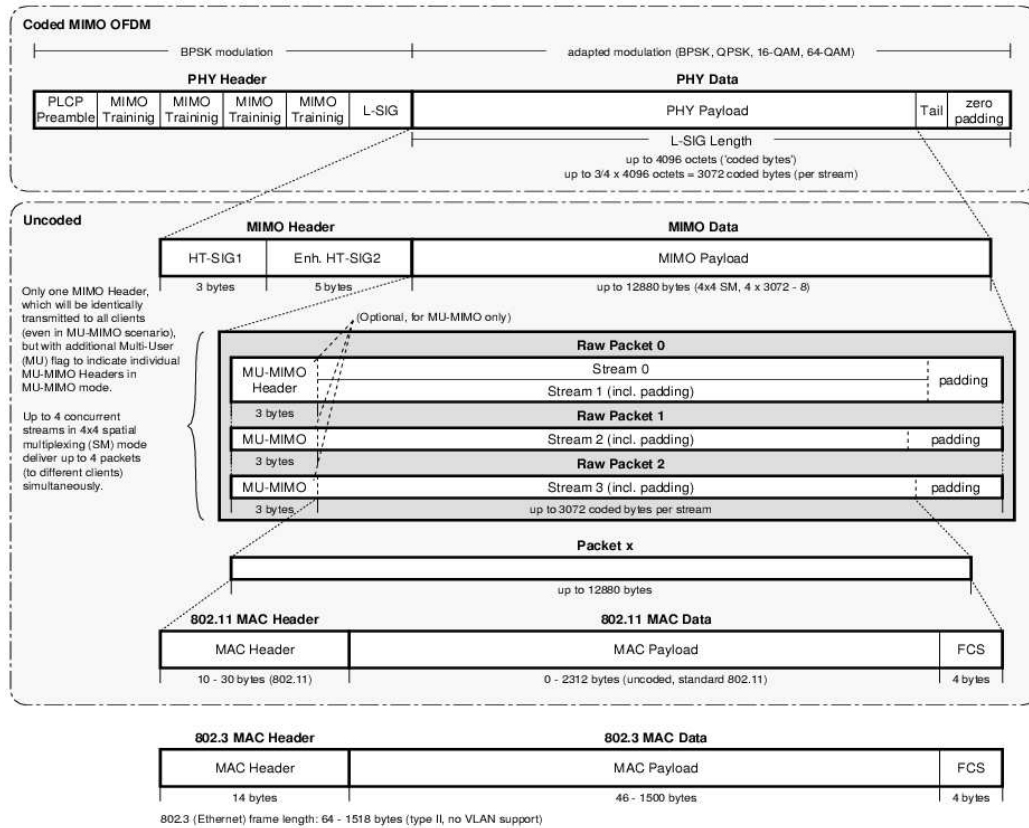


Figure 2.8: Summary of the PHY-layer frame structure to be used for the initial MU-MIMO testbed

2.4 Non Real-Time MU-MIMO Testbed

For the testing of MU-MIMO PHY layer algorithms and transmission schemes, a simplified PHY-layer testbed with offline processing using MATLAB is developed. The corresponding hardware is based on the RF subsystem and on the associated FPGA interface board used for the real-time MU-MIMO testbed (cf. Fig. 2.6).

The baseband samples to be transmitted are provided by a host-PC through a USB interface and are stored in the FPGAs internal and in the carrier boards external memories. When an entire frame is available to the FPGA, the baseband samples are upsampled to a sampling rate of 20 MHz or 40 MHz and are sent to the RF boards. The receivers are synchronized with the transmitter either through a cable or through a basic preamble which can be detected through a matched filter on the receivers FPGA. The received baseband samples are then stored again in memory and are transferred through the USB interface to the host-PC for offline processing/decoding.

Chapter 3

Testbed Extension Summary and Roadmap

A summary of the testbed infrastructure to be used within MASCOT is provided in Tbl. 3.1. The corresponding milestones and planned dates of delivery are also given in the table. Note that the date of delivery for M2.3.1 has been postponed by two months compared to the original proposal. A list of tasks performed since the start of the project and the planning for the tasks remaining to achieve the proposed milestones are provided in the next section.

Table 3.1: Overview of the evolution of the MU-MIMO testbed infrastructure to be developed/used within MASCOT

	ETH Testbed	MASCOT		
		Phase-1a	Phase-2	Phase-1b
Delivery Milestone		31.7.2007 M2.3.1	31.12.2007 M2.3.2	31.7.2007 M2.3.1
Antenna Config.	4×4			
Modulation	MIMO-OFDM			MIMO
PHY-DSP	Real-time FPGA			Offline MATLAB
RF	discrete	integrated		
# of terminals	2	3	5	5
# of FPGAs	1	2+1	2+1	1
Logic cells	76.8K	161.5K	339.3K	55.3K
DSP resources	168	976	896	512
Connection type	point-to-point	point-to-multipoint		
	unidirectional	bidirectional		unidirectional

3.1 Tasks and Milestones

MU-MIMO OFDM Testbed Extensions (M2.3.1) Tbl. 3.2 lists the key work items for the extension of the ETHZ MIMO-OFDM testbed to support the development of a MU-MIMO demonstrator.

Table 3.2: Workplan for extension of the ETHZ MIMO-OFDM testbed

Task	Status	Deadline
MIMO-OFDM PHY implementation	Complete	
Integrated SISO RF	Complete	
Integrated MIMO RF	Complete	
Baseband/RF integration	In progress	25.5.2007
PHY/MAC system architecture	Complete	
PHY/MAC integration	In progress	20.6.2007
Replication of MIMO RF	In progress	1.6.2007
Implementation of 3-terminal demonstration	To be done	31.7.2007

Offline processing MU-MIMO Testbed Tbl. 3.3 lists the tasks required for setting up a MU-MIMO testbed and a demonstration of different STBCs with real-time transmission and offline processing in MATLAB.

Table 3.3: Workplan for building a MU-MIMO PHY-layer testbed with offline processing

Task	Status	Deadline
Design FPGA platform	Complete	
Replication of FPGA platform	To be done	1.6.2007
MATLAB interface implementation	In progress	15.7.2007
STBC MATLAB simulations	In progress	1.6.2007
Implementation of STBC demonstration	To be done	1.7.2007

MU-MIMO OFDM Demonstration (M2.3.2) Tbl. 3.3 lists the tasks required and the expected completion dates for a real-time demonstration and for initial measurements using the MASCOT real-time MU-MIMO testbed.

Table 3.4: Workplan for the demonstration of the MU-MIMO testbed

Task	Status	Deadline
FPGA platform architecture	Complete	
Schematic entry and layout	To be done	15.7.2007
FPGA platform production	To be done	1.9.2007
Implement PHY/MAC on revised platform	To be done	1.10.2007
Definition of the MU-MIMO demonstration	To be done	1.7.2007
MU-MIMO MAC specification	To be done	1.8.2007
MU-MIMO MAC development	To be done	1.12.2007
MU-MIMO measurements	To be done	14.12.2007

3.2 Risk Analysis

Milestone M2.3.1 provides the basis for the extension of the testbed to a MU-MIMO system. Any delays in this milestone will put more pressure on achieving the milestone M2.3.2 which corresponds to the first demonstration of a MU-MIMO system. However, since all components of the setup have already been tested individually (especially the boards) delays due to major functional problems in any of the components of the system are unlikely. A bottle neck is the fabrication of the RF subsystem for which currently only 2 boards have been populated. However, we expect that the remaining boards can be completed in time. Moreover, such a delay would not influence the time line of the work ahead and is thus not critical.

To further minimize the risks associated with delays in the design process of the extremely complex real-time system, a demonstrator with non real-time processing has been added to the testbed infrastructure. This setup will allow to test PHY layer algorithms and coding schemes under real-world conditions with a minimum effort since signal processing can be implemented in software on a host-PC. Relevant results can initially be demonstrated using this platform. Hence delayed migration of the real-time platform does not hinder progress in the demonstration of MU-MIMO algorithms over real-world channels.

The main risks associated with the timely delivery of M2.3.2 are delays in the redesign process of the VAMP2 platform, underestimation of the effort required for the implementation of a MU-MIMO demonstration and a lack of processing resources on the hardware platform. The first point is mitigated by outsourcing the design of the VAMP2 platform to an experienced company. To minimize risks associated with the MAC layer developments, a MAC software expert will be joining the team at ETH in June 2007. Risks associated with resource constraints of the prototyping platform are mitigated by using

top-of-the-line devices for the VAMP2 platform and by providing provisions to put the PHY layer design on an ASIC leaving all FPGA resources to be used by the MAC layer.

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